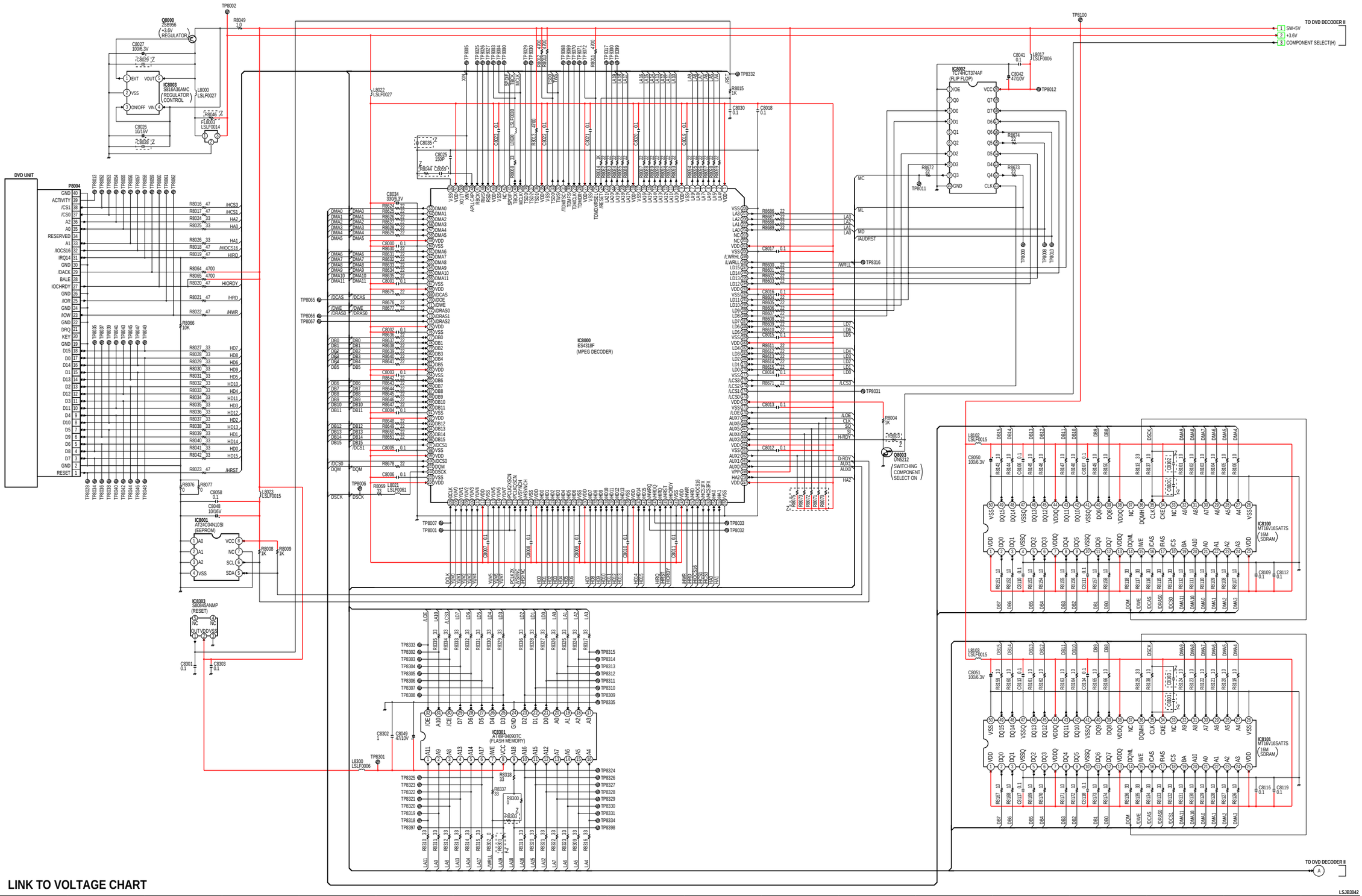
DVD DECODER I SCHEMATIC DIAGRAM

NOTE:
PARTS ENCLOSED IN DASHED LINES MARKED "Z" ARE NOT USED.

NOTE:
FOR SCHEMATIC DIAGRAM AND CIRCUIT BOARD LAYOUT NOTES, REFER TO BEGINNING OF SCHEMATIC SECTION.



I/O CHART OF IC8000

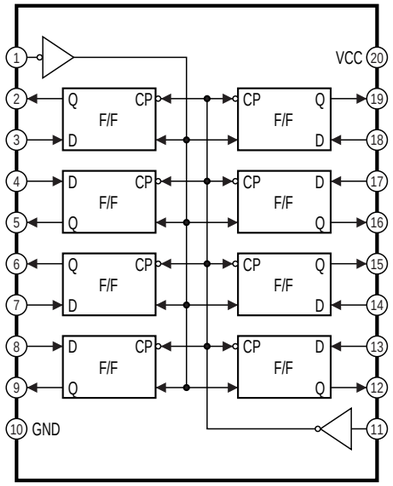
Pin No.	I/O	Signal Name	Description
1	I	VDD	+3.6V
2	O	LA4	Memory address 4
3	O	LA5	Memory address 5
4	O	LA6	Memory address 6
5	O	LA7	Memory address 7
6	O	LA8	Memory address 8
7	O	LA9	Memory address 9
8	-	VSS	Ground
9	I	VDD	+3.6V
10	O	LA10	Memory address 10
11	O	LA11	Memory address 11
12	O	LA12	Memory address 12
13	O	LA13	Memory address 13
14	O	LA14	Memory address 14
15	O	LA15	Memory address 15
16	O	LA16	Memory address 16
17	-	VSS	Ground
18	I	VDD	+3.6V
19	O	LA17	Memory address 17
20	O	LA18	Memory address 18
21	O	LA19	Memory address 19
22	O	LA20	Memory address 20
23	O	LA21	Memory address 21
24	I	/RESET	Reset : low
25	-	TDMDX/RSEL	(Not used)
26	-	VSS	Ground
27	I	VDD	+3.6V
28	-	TDMDR	(Not used)
29	-	TDMCLK	(Not used)
30	-	TDMFS	(Not used)
31	-	/TDMTSC	(Not used)
32	O	TWS	Audio transmit frame sync
33	O	TSD0	Audio serial data
34	-	VSS	Ground
35	I	VDD	+3.6V
36	-	TSD1	(Not used)
37	-	TSD2	(Not used)
38	-	TSD3	(Not used)
39	I/O	MCLK	Audio master clock
40	I/O	TBCK	Audio transmit bit clock
41	O	SPDIF	IEC958 audio data
42	-	NC	(Not used)
43	-	VSS	Ground
44	I	VDD	+3.6V
45	-	RSD	(Not used)
46	-	RWS	(Not used)
47	-	RBCK	(Not used)
48	-	APLLCAP	(Not used)
49	I	XIN	27MHz clock
50	-	XOUT	(Not used)
51	I	VDD	+3.6V
52	-	VSS	Ground
53	O	DMA0	SDRAM address 0
54	O	DMA1	SDRAM address 1
55	O	DMA2	SDRAM address 2
56	O	DMA3	SDRAM address 3
57	O	DMA4	SDRAM address 4
58	O	DMA5	SDRAM address 5
59	I	VDD	+3.6V

Pin No.	I/O	Signal Name	Description
60	-	VSS	Ground
61	O	DMA6	SDRAM address 6
62	O	DMA7	SDRAM address 7
63	O	DMA8	SDRAM address 8
64	O	DMA9	SDRAM address 9
65	O	DMA10	SDRAM address 10
66	O	DMA11	SDRAM address 11
67	-	VSS	Ground
68	I	VDD	+3.6V
69	O	/DCAS	Column address strobe : low
70	-	/DOE	(Not used)
71	O	/DWE	Write enable : low
72	O	/DRAS0	Row address strobe : low
73	-	/DRAS1	(Not used)
74	-	/DRAS2	(Not used)
75	I	VDD	+3.6V
76	-	VSS	Ground
77	I/O	DB0	SDRAM data 0
78	I/O	DB1	SDRAM data 1
79	I/O	DB2	SDRAM data 2
80	I/O	DB3	SDRAM data 3
81	I/O	DB4	SDRAM data 4
82	I/O	DB5	SDRAM data 5
83	I	VDD	+3.6V
84	-	VSS	Ground
85	I/O	DB6	SDRAM data 6
86	I/O	DB7	SDRAM data 7
87	I/O	DB8	SDRAM data 8
88	I/O	DB9	SDRAM data 9
89	I/O	DB10	SDRAM data 10
90	I/O	DB11	SDRAM data 11
91	-	VSS	Ground
92	I	VDD	+3.6V
93	I/O	DB12	SDRAM data 12
94	I/O	DB13	SDRAM data 13
95	I/O	DB14	SDRAM data 14
96	I/O	DB15	SDRAM data 15
97	O	/DCS1	SDRAM chip select : low
98	-	VSS	Ground
99	I	VDD	+3.6V
100	O	/DCS0	SDRAM chip select : low
101	O	DQM	Data input/output mask
102	O	DSCK	SDRAM clock
103	-	VSS	Ground
104	I	VDD	+3.6V
105	I	DCLK	27MHz clock
106	O	YUV0	YUV data 0
107	O	YUV1	YUV data 1
108	O	YUV2	YUV data 2
109	O	YUV3	YUV data 3
110	O	YUV4	YUV data 4
111	I	VDD	+3.6V
112	-	VSS	Ground
113	I	YUV5	YUV data 5
114	I	YUV6	YUV data 6
115	I	YUV7	YUV data 7
116	I	PCLK2XSCN	2X pixel clock
117	I/O	PCLKQSCN	pixel clock
118	I/O	/VSYNCH	V-sync signal

Pin No.	I/O	Signal Name	Description
119	I/O	/HSYNCH	V-sync signal
120	-	VSS	Ground
121	I	VDD	+3.6V
122	I/O	HD0	Host data 0
123	I/O	HD1	Host data 1
124	I/O	HD2	Host data 2
125	I/O	HD3	Host data 3
126	I/O	HD4	Host data 4
127	I/O	HD5	Host data 5
128	I/O	HD6	Host data 6
129	-	VSS	Ground
130	I	VDD	+3.6V
131	I/O	HD7	Host data 7
132	I/O	HD8	Host data 8
133	I/O	HD9	Host data 9
134	I/O	HD10	Host data 10
135	I/O	HD11	Host data 11
136	I/O	HD12	Host data 12
137	I/O	HD13	Host data 13
138	-	VSS	Ground
139	I	VDD	+3.6V
140	I/O	HD14	Host data 14
141	I/O	HD15	Host data 15
142	-	/HWRQ	(Not used)
143	-	/HRDQ	(Not used)
144	I/O	HIRQ	Host interrupt
145	I	/HRST	Host reset : low
146	I	HIORDY	Host I/O ready
147	-	VSS	Ground
148	I	VDD	+3.6V
149	O	/HWR	Host write request : low
150	I	/HRD	Host read request : low
151	I	/HIOCS16	Device 16-bit data transfer
152	O	/HCS1FX	Host select 1
153	O	/HCS3FX	Host select 3
154	I/O	HA0	Host address 0
155	I/O	HA1	Host address 1
156	-	VSS	Ground
157	I	VDD	+3.6V
158	I/O	HA2	Host address 2
159	I	VPP	Peripheral protection voltage
160	I/O	AUX0	I2C serial data
161	I	AUX1	I2C serial clock
162	O	AUX2	DVD ready (Busy : low)
163	-	VSS	Ground
164	I	VDD	+3.6V
165	-	AUX3	(Not used)
166	I	AUX4	DVD chip select : low
167	O	AUX5	Serial data 1
168	I	AUX6	Serial data 0
169	I	AUX7	Serial clock
170	O	/LOE	Output enable : low
171	-	VSS	Ground
172	I	VDD	+3.6V
173	-	/LCS0	(Not used)
174	-	/LCS1	(Not used)
175	O	/LCS2	Clock
176	O	/LCS3	Memory chip select : low
177	-	VSS	Ground

Pin No.	I/O	Signal Name	Description
178	I/O	LD0	Memory data 0
179	I/O	LD1	Memory data 1
180	I/O	LD2	Memory data 2
181	I/O	LD3	Memory data 3
182	I/O	LD4	Memory data 4
183	I	VDD	+3.6V
184	-	VSS	Ground
185	I/O	LD5	Memory data 5
186	I/O	LD6	Memory data 6
187	I/O	LD7	Memory data 7
188	I/O	LD8	Memory data 8
189	I/O	LD9	Memory data 9
190	I/O	LD10	Memory data 10
191	I/O	LD11	Memory data 11
192	-	VSS	Ground
193	I	VDD	+3.6V
194	I/O	LD12	Memory data 12
195	I/O	LD13	Memory data 13
196	I/O	LD14	Memory data 14
197	I/O	LD15	Memory data 15
198	O	/LWRLL	Write enable : low
199	-	/LWRHL	(Not used)
200	-	VSS	Ground
201	I	VDD	+3.6V
202	-	NC	(Not used)
203	-	NC	(Not used)
204	O	LA0	Memory address 0
205	O	LA1	Memory address 1
206	O	LA2	Memory address 2
207	O	LA3	Memory address 3
208	-	VSS	Ground

IC8002 DETAIL BLOCK DIAGRAM



I/O CHART OF IC8301

Pin No.	I/O	Signal Name	Description
1	I	A11	Memory address 11
2	I	A9	Memory address 9
3	I	A8	Memory address 8
4	I	A13	Memory address 13
5	I	A14	Memory address 14
6	I	A17	Memory address 17
7	I	/WE	Write enable : low
8	I	VCC	+5.0V
9	I	A18	Memory address 18
10	I	A16	Memory address 16
11	I	A15	Memory address 15
12	I	A12	Memory address 12
13	I	A7	Memory address 7
14	I	A6	Memory address 6
15	I	A5	Memory address 5
16	I	A4	Memory address 4
17	I	A3	Memory address 3
18	I	A2	Memory address 2
19	I	A1	Memory address 1
20	I	A0	Memory address 0
21	I/O	D0	Memory data 0
22	I/O	D1	Memory data 1
23	I/O	D2	Memory data 2
24	-	GND	Ground
25	I/O	D3	Memory data 3
26	I/O	D4	Memory data 4
27	I/O	D5	Memory data 5
28	I/O	D6	Memory data 6
29	I/O	D7	Memory data 7
30	I	/CE	Memory chip select : low
31	I	A10	Memory address 10
32	I	/OE	Output enable : low

I/O CHART OF IC8100/IC8101

Pin No.	I/O	Signal Name	Description
1	I	VDD	+3.6V
2	I/O	DQ0	SDRAM data 7
3	I/O	DQ1	SDRAM data 6
4	-	VSSQ	Ground
5	I/O	DQ2	SDRAM data 5
6	I/O	DQ3	SDRAM data 4
7	-	VDDQ	+3.6V
8	I/O	DQ4	SDRAM data 3
9	I/O	DQ5	SDRAM data 2
10	-	VSSQ	Ground
11	I/O	DQ6	SDRAM data 1
12	I/O	DQ7	SDRAM data 0
13	I	VDDQ	+3.6V
14	I	DQML	Data input/output mask
15	I	/WE	Write enable : low
16	I	/CAS	Column address strobe : low
17	I	/RAS	Row address strobe : low
18	I	/CS	SDRAM chip select : low
19	I	BA	SDRAM address 11
20	I	A10	SDRAM address 10
21	I	A0	SDRAM address 0
22	I	A1	SDRAM address 1
23	I	A2	SDRAM address 2
24	I	A3	SDRAM address 3
25	I	VDD	+3.6V
26	-	VSS	Ground
27	I	A4	SDRAM address 4
28	I	A5	SDRAM address 5
29	I	A6	SDRAM address 6
30	I	A7	SDRAM address 7
31	I	A8	SDRAM address 8
32	I	A9	SDRAM address 9
33	-	NC	(Not used)
34	-	CKE	(Not used)
35	I	CLK	SDRAM clock
36	I	DQMH	Data input/output mask
37	-	NC	(Not used)
38	I	VDDQ	+3.6V
39	I/O	DQ8	SDRAM data 8
40	I/O	DQ9	SDRAM data 9
41	-	VSSQ	Ground
42	I/O	DQ10	SDRAM data 10
43	I/O	DQ11	SDRAM data 11
44	-	VDDQ	+3.6V
45	I/O	DQ12	SDRAM data 12
46	I/O	DQ13	SDRAM data 13
47	-	VSSQ	Ground
48	I/O	DQ14	SDRAM data 14
49	I/O	DQ15	SDRAM data 15
50	-	VSS	Ground

I/O CHART OF IC8001

Pin No.	I/O	Signal Name	Description
1	-	A0	(Not used)
2	-	A1	(Not used)
3	-	A2	(Not used)
4	-	VSS	Ground
5	I/O	SDA	I2C Serial data
6	O	SCL	I2C Serial clock
7	-	NC	(Not used)
8	I	VCC	+5.0V

I/O CHART OF IC8403

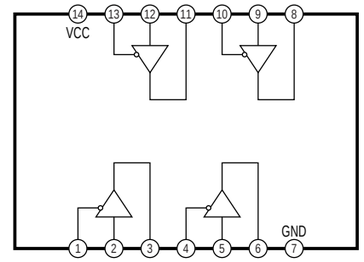
Pin No.	I/O	Signal Name	Description
1	I	XTI	27MHz clock
2	O	SCKO	System clock
3	I	VCP	+5.0V
4	-	NC	(Not used)
5	-	MCKO	(Not used)
6	I	ML	Mode control latch
7	I	MC	Mode control clock
8	I	MD	Mode control data
9	I	RSTB	Audio DAC reset : low
10	-	ZERO	(Not used)
11	O	V OUT R	Audio R-CH
12	-	GNDA	Ground
13	I	VCA	+5.0V
14	O	V OUT L	Audio L-CH
15	-	CAP	Audio common
16	I	BCKIN	Audio bit clock
17	I	DIN	Audio serial data
18	I	LRCIN	Audio left/right clock
19	-	NC	(Not used)
20	-	RSV	(Not used)
21	I	VDD	+5.0V
22	-	GNDD	Ground
23	-	GNDP	Ground
24	-	XTO	(Not used)

DVD DECODER II SCHEMATIC DIAGRAM

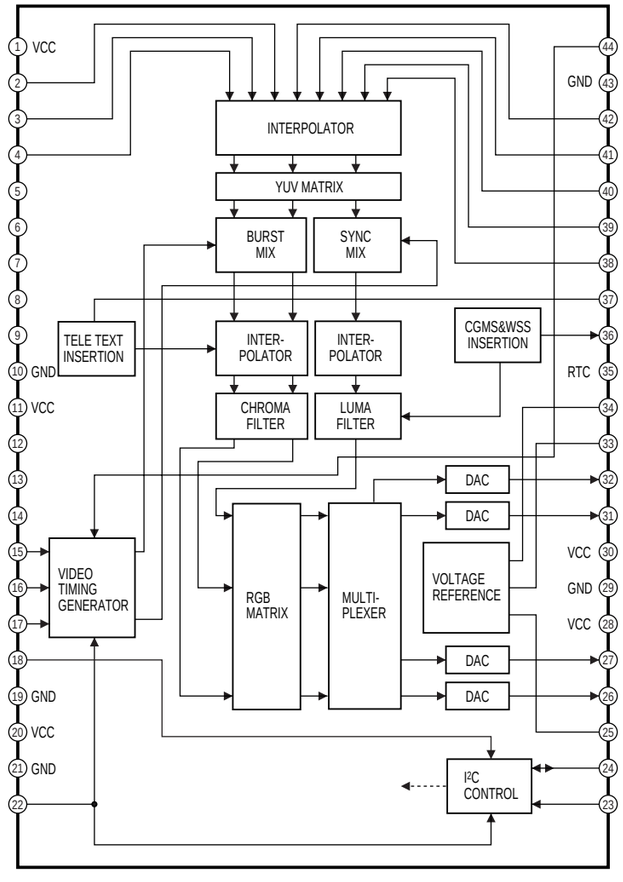
NOTE:
PARTS ENCLOSED IN DASHED LINES MARKED "Z" ARE NOT USED.

NOTE:
FOR SCHEMATIC DIAGRAM AND CIRCUIT BOARD LAYOUT NOTES, REFER TO BEGINNING OF SCHEMATIC SECTION.

IC8502 DETAIL BLOCK DIAGRAM



IC8200 DETAIL BLOCK DIAGRAM



LINK TO VOLTAGE CHART

LSJB3042